REMARKS

Claims 1 to 20 are pending. Claims 1 and 11 are independent.

Compliance with 35 U.S.C. §103

The Office Action cites Arndt et al. (US 2005/0018669 A1) and Franke et al. (US 6542513) and alleges that the pending claims are obvious in light of the combination of Arndt et al. and Franke et al.

The Applicants submit that this is incorrect at least because:

- claim 1 recites " a full-duplex packetized interconnect directly connecting a CPU of the first compute node to a network interface connected to the inter-node communication network"; and
- claim 11 recites "a dedicated full-duplex packetized interconnect directly coupling the CPU to the network interface".

As explained in detail below, the cited references, as understood, fail to disclose or suggest these features in the contexts of claims 1 and 11 respectively.

Arndt et al., as understood, discloses a system area network (SAN) having a number of host processor nodes (102, 104) interconnected by a switched communication fabric (116). Each host processor node has host communication adapters (HCA 118, 120, 122, 124). Figure 1 shows structure of host processor nodes (102, 104). Notably, internal to each node, each HCA is connected to memory (132, 142).

Claims 1 and 11

Claim 1 recites an interconnect "directly connecting a CPU of the first compute node to a network interface connected to the inter-node communication network". Claim 11 recites an interconnect directly coupling the CPU to the network interface. The Applicants submit that Arndt fails to disclose these features of claims 1 and 11. Arndt fails to show any interconnect directly connecting each HCA to a CPU (126, 128, 130, 136, 138, 140).

The Office Action incorrectly indicates that these features are described in paragraphs [0034] and [0037] of Arndt et al. Paragraph [0034] describes links of switched communications fabric (116). This paragraph does not relate to or describe the internal structure of a node.

Paragraph [0037] states that "Host processor node 104 contains host channel adapter 122 and host channel adapter 124. Host processor node 104 also includes central processing units 126-130 and a memory 132 interconnected by a bus system 134." Paragraph [0037] gives no details of the construction of bus system 134. Paragraph [0037] expressly states that the bus system interconnects the central processing units and memory. The features being discussed in paragraph [0037] are shown in Figure 1. As noted above, Figure 1 shows that HCA 122 and 124 are connected to memory 132 and are not directly connected to any one of processing units 126-130.

Franke et al. does not remedy the defects of Arndt et al. Franke et al, as understood, discloses computer systems that include processors (12) or end nodes (18). Franke et al., as understood, does not disclose or suggest the above-noted features of claims 1 and 11.

In addition, claims 1 and 11 each recite that the interconnect is a "`full-duplex packetized interconnect`". The Examiner's attention is drawn to the definition of 'packetized interconnect' in paragraph [0020] of the present application which includes: "Interconnects which use memory access semantics including packetized parallel interconnects having a number of signal lines which is smaller than a width of data words being transferred and packetized serial interconnects are referred to herein as 'packetized interconnects'".

Arndt et al. describes bus systems (134, 144) that interconnect central processing units and a memory in each host processor node. Arndt et al.. as understood, does not describe any particular characteristics of bus systems (133, 134) and in particular do not indicate that bus systems (134, 144) provide "`full-duplex packetized`" interconnects as claimed in each independent claim. Franke et al. fails to remedy this defect.

Therefore, claims 1 and 11 are submitted to be patentable over the cited combination of Arndt et al. and Franke et al.

Claims 2 and 12

In addition, claim 2 recites that "the network interface and the CPU are the only devices configured to place data on the packetized interconnect" and claim 12 recites that "the dedicated packetized full-duplex interconnect is not shared by any devices other than the CPU and the network interface". The Applicants submit that these features are not disclosed or suggested by the Arndt et al. / Franke et al. combination. In Arndt et al., bus systems (134, 144) are each shared by multiple processors and a memory. Arndt et al., as understood, does not show an interconnect having the features of claim 2 or 12. Franke et al. does not remedy this deficiency.

The Applicants submit that the Office Action is incorrect wherein it indicates that the features of claims 2 and 12 are disclosed by Arndt et al. in paragraphs [0047], [0048] and [0053]. None of these paragraphs disclose an interconnect directly connecting a CPU to a network interface or disclose that such an interconnect is 'not shared' as in claim 12 or that "the network interface and the CPU are the only devices configured to place data on the packetized interconnect" as in claim 2.

Therefore, claims 2 and 12 and the claims that depend from claims 2 and 12 are submitted to further distinguish the cited references.

Claims 5 and 19

Claim 5 recites "at the network interface, determining a size of the data and, based upon the size of the data, selecting among two or more protocols for transmitting the data". Claim 19 recites "the network interface comprises a facility configured to determine a size of data to be transmitted to another compute node and, based upon the size, to select among two or more protocols...". The Office Action appears to be attempting to equate the four types of transport services referenced in paragraph [0068] to the claimed 'two or more protocols". Applicants point out that the transport services referred to in paragraph [0068] of Arndt et al. are assigned when a queue pair is created (see first sentence of paragraph [0067]). Claims 5 and 19 recite that protocol

selection is "based upon the size of the data". Arndt et al., as understood, do not disclose selecting among the transport services discussed in paragraph [0068] based upon the size of any data.

Therefore, claims 5 and 19 and the claims that depend from claims 5 and 19 are submitted to further distinguish the cited references.

Claim 17

Claim 17 recites " A compute node ... comprising a plurality of CPUs each connected to the interface by a separate dedicated full-duplex packetized interconnect." Applicants submit that this feature is not disclosed by either of Arndt et al. or Franke et al., as understood. Arndt et al., as understood discloses that all processors are interconnected by a bus system (134, 144). Franke et al. does not remedy this defect.

Therefore claim 17 is submitted to be patentable over the cited combination of Arndt et al. and Franke et al.

Claim 18

Claim 18 recites "the CPU is connected to each of a plurality of network interfaces by a plurality of dedicated full-duplex packetized interconnects". As discussed above, Arndt et al. does not disclose a CPU connected to even one network interface by a dedicated full-duplex packetized interconnect. Arndt et a., as understood, fails to disclose the feature of claim 18. Franke et al., as understood, also fails to describe or suggest the feature of claim 18.

Therefore claim 18 is submitted to be patentable over the cited combination of Arndt et al. and Franke et al.

Conclusion

The Applicants submit that the comments above address all issues raised in the Office Action and that claims 1 to 20 are in condition for allowance. Reconsideration and allowance of this application is respectfully requested.

Respectfully submitted,

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